

The Examiner rejected Claims 22-29, 31 and 33-34 of the present application under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 1-18 of US Patent No. 6,392,256. The Examiner stated that with respect to Claim 22 of the present application, the claims of the '256 patent discloses an optical transmitter and receiver pair having a semiconductor substrate, an optical transmitter formed on the substrate, an optical receiver formed adjacent to the optical transmitter and an isolation area. However, the claims in the '256 patent are directed to one embodiment of the invention wherein a substrate is provided wherein a VCSEL (optical transmitter) structure is formed over the entire surface of the substrate. The optical receiver portion is then formed on top of the VCSEL layers. To prevent interference between the bottom layers of the VCSEL and the optical receiver layers formed thereon, a proton injection region is introduced into the VCSEL around the photo receiver to render the underlying VCSEL layers inactive, thereby preventing electrical interference between the two devices. In the '256 patent the claimed structure is clearly a stacked arrangement.

In contrast, the present application is directed to a substrate having an optical transmitter structure (VCSEL) formed on a portion thereof and an optical receiver formed laterally adjacent to (beside) the VCSEL not on top as in the '256 patent. Further, Claim 22 includes a limitation that the VCSEL and optical receiver be optically isolated from one another. It is clear in Claim 22, as amended, that the present invention is not directed to a stacked configuration. The distinction can be seen by comparing Figs. 3 and 5. The claims in the present invention are directed to the embodiment shown in Fig. 3 where a substrate 60 is provided on which a VCSEL 89 is formed in one area and a photo receiver 62 is formed in another adjacent area. The isolation area 80 is provided to eliminate any electrical or potential optical interference from traveling through the substrate 60 and disrupting the photo receiver 62. In contrast, the claims in the '256 patent are directed to the embodiment in Fig. 5 where a substrate structure 78 is provided wherein the entire surface is coated with a built-up VCSEL layered construction 76. The photo detector region 90 is then applied on top of the VCSEL layers 76. Isolation areas 80 are then created by injecting a proton stream into the VCSEL layers 76 around the area upon which the photo detector 90 is constructed to selectively inactivate the VCSEL 76 in this area by preventing the flow of electricity. The additional

drawback in the '256 invention is that the inactive VCSEL 76 may accidentally become activated and provide optical interference into the back of the photoreciever 62. In order to prevent this a reverse pass diode must be formed in the structure of the VCSEL 76 below the photo reciever 62 to eliminate the potential of activation.

It is clear from this comparison that the claims of the present application and the claims of the '256 patent are directed to two distinctly different constructions. As a result, the claims of the present application as amended are directed to an invention that is patentably distinct from the invention disclosed in the '256 patent.

In the alternative, should the Examiner determine that there is insufficient structural differences between the invention of the present application and the invention disclosed in the '256 patent to warrant a patentable distinct embodiment, the Applicant will be willing to file a Terminal Disclaimer in addition to paying the appropriate fee if required.

### III. REJECTION OF CLAIMS UNDER 35 USC 102

Claims 1-26, 28-29, 32 and 34-358-9 were rejected under 35 USC 102(e), as being anticipated by US Patent No. 5,266,794 (Olbright et al.). The Examiner stated that with regard to Claim 22, Olbright discloses an integrated light emitting and photo detector device including a semiconductor substrate, an optical transmitter on the substrate and an optical receiver formed laterally adjacent to the optical transmitter. The device, however, as described in the disclosure relative to Fig. 8, is formed to become a single switch module in a three dimensional switching array. The photo detector section is formed to work in interlocked relation to the VCSEL section by communicating through the substrate and in particular by communicating through the semiconductor substrate having logic etched thereon. The photo detector is specially formed to receive light signals from both the front and the back. In addition, the VCSEL includes a HBT/HPT photo detector base upon which it is built. In this manner, the construction allows the module to receive and process incoming signals from three different points. In response to this input, the module will then selectively repeat the incoming signal using the VCSEL portion of the module. It is a critical component of the disclosure that the photo detector and VCSEL be allowed to communicate. It is also clear from the disclosure that the photo detector and VCSEL sections must be separated by a relatively large distance to

prevent interference between signals received at the rear of the photo detector and signals received at the rear of the VCSEL. If these two components were placed too closely on the substrate, cross talk and poor switching results would be produced.

In contrast, the present invention specifically provides a critical electrical isolation region between the receiver and transmitter sections to electrically isolate them from one another. This isolation region is in the form of a proton injected area in the substrate that prevents electrical conductivity across the region. In this manner, while both the transmitter and receiver are mounted onto the same substrate, they are electrically isolated from one another allowing completely independent operation. This is the feature of the present invention that allows the module to be used for simultaneous TX/RX operations in the high-speed transfer of data over paired fiber runs. Further, this isolation area allows the transmitter and receiver to be formed more closely to one another on the substrate, while preventing cross talk and interference between the two parts of the module. This feature of the present invention is important to allow the module to be employed with dual mode fibers, where two fiber conductors, separated by only 250 microns, are bundled together into a single core and jacket. This close spacing between the transmitter and receiver was previously unattainable in the prior art.

Since the present invention specifically recites subject matter that is not disclosed in Olbright, the rejection is not believed to be applicable. Specifically, since Olbright does not disclose the provision of electrical isolation between the transmitter and receiver sections of the module to allow independent operation of the two units, the disclosure in Olbright cannot anticipate the invention of the present application. Therefore, reconsideration and withdrawal of this rejection is respectfully solicited.

#### IV. REJECTION OF CLAIMS UNDER 35 USC 103

Claims 30-31 were rejected under 35 USC 103(a) as being unpatentable over Olbright in view of US Patent No. 5,136,603 (Hasnain et al.). The Examiner has stated that as applied above Olbright discloses the present invention with the exception of an intrinsic layer in the photodiode to provide an improved PIN type diode that enhances the confinement of the carriers. The Examiner further stated that since Hasnain discloses the use of PIN type photo diodes, it would have been obvious to one skilled in the art to combine the references to render the present invention obvious.

As stated above, with respect to Olbright, the combination of these two references is devoid of any teaching regarding the isolation of the two components in the module. There is no teaching either alone or in combination of these cited references that provides for the placement in close proximity of the photodiode and VCSEL portions of the module through the use of a proton injected isolation region. While the use of an improved PIN type photo detector does allow the two components to be placed more closely to one another, without the required isolation area, the present invention would suffer from a high degree of cross talk and interference rendering it ineffective.

Since the references cited by the Examiner cannot be combined to arrive at the invention of the present application, is not believed that the present invention is rendered obvious in view of the combination. Therefore, the Applicant requests withdrawal of this rejection.

Claims 27-33 were rejected under 35 USC 103(a) as being unpatentable over Olbright in view of US Patent No. 5,498,883 (Lebby et al.). The Examiner has stated that as applied above Olbright discloses the present invention with the exception of cladding layers on the top and bottom of the active layer in the VCSEL to improve the confinement of the carriers. The Examiner further stated that since Lebby discloses the use of cladding and anti-reflective layers in VCSELS, it would have been obvious to one skilled in the art to combine the references to render the present invention obvious.

As stated above in the comments related to Olbright alone, the device in Olbright provides for a module that includes a photo detector and a VCSEL that are designed to work in conjunction with one another to receive and process signals from both the front and rear sides of the substrate that are then processed to activate the VCSEL to relay the signal as necessary. Should one skilled in the art apply the cladding layers described in Lebby to the Olbright disclosure, the present invention would still not be disclosed. The present invention includes specific isolation limitations that restrict both electrical and optical interference that are not disclosed in the cited prior art that allow the two elements, namely the transmitter and receiver, mounted in close proximity on the module to function entirely independent of one another.

Since the references cited by the Examiner cannot be combined to arrive at the invention of the present application, is not believed that the present invention is rendered

Serial No. 09/484,348

obvious in view of the combination. Therefore, the Applicant requests withdrawal of this rejection.

Since the references cited by the Examiner cannot be combined to arrive at the invention of the present application, is not believed that the present invention is rendered obvious in view of the combination. Therefore, the Applicant requests withdrawal of these grounds for rejection.

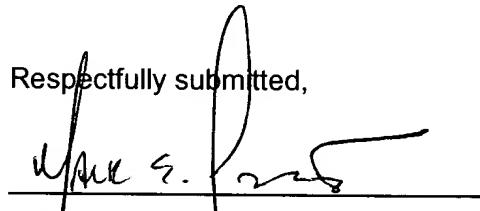
V. CONCLUSION

Accordingly, claims 22-39 are believed to be in condition for allowance and the application ready for issue.

Corresponding action is respectfully solicited.

PTO is authorized to charge any additional fees incurred as a result of the filing hereof or credit any overpayment to our account #02-0900.

Respectfully submitted,

  
\_\_\_\_\_  
Mark E. Tetreault, Esq.  
Reg. No. 48,289

BARLOW, JOSEPHS & HOLMES, Ltd.  
101 Dyer Street, 5<sup>th</sup> Floor  
Providence, RI 02903  
(401) 273-4446 (tel)  
(401) 273-4447 (fax)  
[met@barjos.com](mailto:met@barjos.com)

#9/Sub Spec.  
(NE)  
2.11.03  
C. Moore

### ATTACHMENT A

Amended specification with markings to show the revisions made.

### DETAILED DESCRIPTION OF THE INVENTION

The present invention generally pertains to a monolithic semiconductor device having a VCSEL integrated with a photodetector on the same substrate, wherein the VCSEL and photodetector are to be operated independently as [a] transmit and receive devices respectively. The VCSEL and photodetector are physically situated in close enough proximity to permit packaging of one or more pairs of the VCSEL and photodetector such that they may be coupled to multifiber ferrules having fiber spacing on the order of 250 microns or less. The present invention also includes a method of manufacturing the independently operated VCSEL and photodetector, as well as the packaging and coupling of one or more pairs of the integrated VCSEL and photodetector [and their coupling] to multifiber ferrules.

A first preferred embodiment of the invention is now discussed in detail in conjunction with Figures 3 and 4. As shown in Figure 3, a VCSEL and a metal -semiconductor-metal (MSM) photodetector are integrated on the same semi-insulating GaAs substrate 60. The conductance of the semi-insulating substrate 60 is typically between about  $10^{-12}$  and  $10^{-5}$  ohm-cm. The VCSEL is built on top of the substrate 60 beginning with an n- layer 68, upon which an n+ layer 70 is grown [which forms] to form the cathode of the VCSEL.

A first mirror 78 is formed on n+ layer 70, which is preferably an epitaxially formed distributed Bragg reflector (DBR) which comprises a plurality of alternating semiconductor layers having high and low indices of refraction, with each layer having a thickness of  $\lambda/4n$ , where  $\lambda$  is the wavelength of the optical radiation emitted from the laser and n is the index of refraction of the layer. The semiconductor layers are doped to achieve n-type conductivity. A quantum well (QW) active region 74 is formed between a first spacer 73 and a second spacer 75, with first spacer 73 formed on the top layer of the first mirror 78. Active region 74 has at least one QW layer.

A second mirror 76 is formed on second spacer 75 and is preferably an epitaxially grown DBR which is comprised of a plurality of alternating semiconductor layers having high and low indices of refraction, with each layer having a thickness of  $\lambda/4n$ , where  $\lambda$  is the wavelength of the optical radiation emitted from the laser and  $n$  is the index of refraction of the layer. The second mirror 76 is doped to achieve p-type conductivity. An isolation implant [80] 81 is formed around the second mirror 76, and preferably extends to a depth just inside spacer 75. A mesa region is then etched around the outside of the VCSEL 89 to a depth that exposes the cathode layer 70. A cathode contact 72 is then formed on the exposed surface of [cathode] n+ layer 70, and an anode contact 82 is formed which overlaps the surface of isolation implant region [80] 81 and the topmost layer of second mirror 76, and which further defines an aperture 88 which comprises a portion of the surface of the top-most layer of second mirror 76. Radiation 84 is emitted through aperture 88.

The MSM photodetector 62 is formed on the surface of the semi-insulating substrate 60 as two non-electrically coupled metal patterns [62] 66 and 64, each having fingers that are interdigitated with one another. When one or both of the patterns is biased to some voltage, carriers generated by received light are swept to the anodes of the two diodes by the applied electric field. Because the MSM 62 operates without conducting any current through the substrate 60, there is virtually no electrical crosstalk or leakage between the VCSEL 89 and the MSM photodetector 62. Thus, the VCSEL 89 can emit radiation 84 from aperture 88 based on digital data to be transmitted while MSM photodetector 62 can receive radiation 86 in which is encoded digital data received from a remote data source. To achieve even better isolation, an isolation region 80 can be formed preferably by proton implant between VCSEL 89 and MSM photodetector 62.

Figure 4 illustrates a plan view of the device that is shown as a cross-section in Figure 3. For clarity, corresponding structures will be indicated by identical index numbers. The [cathode] n+ layer 70 and its metal cathode contact 72 of the VCSEL are extended to the boundary of substrate 60, which is furthest away from MSM photodetector [86] 62. Bond wire 71 can then be used to connect cathode contact 72 to a bond pad of, for example, a lead frame. The VCSEL anode contact 82 is brought to the same substrate boundary by bond wire 77, metal extender 79 and bond wire 69.

Metal patterns 66 and 64, which form the anode and anode terminals of MSM photodetector 62, are also bonded to the leads of whatever form of packaging is used. One of the metal patterns is typically coupled to a bias voltage while the other is coupled to ground or a different bias voltage. An anti reflection coating can be employed on the MSM 62 to increase optical efficiency.

A second preferred embodiment is disclosed in Figure 5a. For convenience and clarity, like structures will be denoted by the same index numbers as in previous figures. This particular embodiment is preferred because it can be implemented using more standard VCSEL manufacturing processes. A first mirror 78 is formed on a standard semiconductor GaAs substrate [79] 60. The first mirror is preferably a semiconductor DBR comprising twenty to thirty periods of AlAs/AlGaAs layers. Each of the layers has a thickness of  $\lambda/(4n)$  and is doped to have n-type conductivity. A first spacer or cladding layer 73 is then formed on first mirror 78, which is either undoped or very lightly doped. An active region 74 is then formed on the first spacer 73, which comprises at least one GaAs QW layer. A second mirror 76 is then formed on top of a second undoped or very lightly doped spacer or cladding layer 75. The second mirror 76 again preferably consists of alternating layers of AlAs/AlGaAs layers, each being  $\lambda/(4n)$  thick. Second mirror 76 is doped to have p-type conductivity. On top of second mirror 76 is formed a thin etch-stop layer 93, which has a significantly higher ratio of Al to Ga, about 9 to 1 or greater. On top of the etch-stop layer 93, an extended p-type layer 100 of AlGaAs is formed. On top of p-type layer 100 is formed an intrinsic layer (i) 102 of undoped GaAs. Finally, an n-type layer 104 is formed on top of intrinsic layer 102.

The structure is then etched in those areas where a VCSEL is to be formed, and not etched where a p-i-n photodiode is to be formed. The etch strips away the n-type layer 104 and intrinsic layer 102 and continues into p-type layer 100 until the etch-stop layer 93 is detected. The etching process is terminated so that the etch-stop layer 93 is etched away and an appropriately thick top layer of second mirror 76 is exposed. Those of skill in the art will recognize that there are other well-known techniques by which the endpoint of an etching process may be detected to end the etching process at the appropriate time and which are intended to be within the scope of the present invention.

A proton isolation implant is performed to create isolation region 80 between VCSEL 92 and p-i-n photodiode 90. The implant region 80 typically achieves a depth, which extends just inside spacer layer 75 and has a width preferably between about 50 and 100 microns. A circular metal contact 82 is then formed on the top of mirror 76 and which overlaps slightly implant region 80. Contact 82 provides access to the anode of VCSEL 92. A contact 81 is then formed on the backside of substrate 79 and serves as the cathode terminal of VCSEL 92. Contacts 94 are preferably formed on both sides of p-i-n photodiode 90 which provide electrical access to the anode of p-i-n photodiode 90 as well as to the anode 98 of the VCSEL 91, which underlies p-i-n photodiode 90. Finally, contact 96 is formed on n-type layer 104 to form the cathode of p-i-n in photodiode 90. An anti-reflection coating preferably having a thickness of about one quarter wavelength is applied to photo-receiving surface 101.

A simplified schematic of the structure of Figure 5a is shown in Figure 5b. VCSEL 92 is operated with forward bias between [anode terminal] contact 82 and cathode terminal 98 to produce radiation 84 having a wavelength of  $\lambda$ . The p-i-n photodiode 90 is operated with reverse bias between cathode contact 96 and anode contacts 94. Moreover, anode contacts 94 are shorted to substrate contact 98 to ensure that VCSEL 91 will not become forward biased and emit light. Thus, VCSEL 92 can be operated to emit light encoded with data to be transmitted to a remote receiver employing a similar structure, and p-i-n photodiode 90 can operate to receive radiation 86, which is encoded with data received from the same remote terminal.

Those of skill in the art will recognize that the exact order in which the process steps take place, as well as the particular material system used, are irrelevant to the patentability of the present invention. For example, one material system might include a GaAs substrate, GaAs quantum wells, DBR layers of AlAs and AlGaAs. Other known material systems may be used to produce different wavelengths of emitted radiation and the particular dimensions of the integrated devices may be changed to suit the particular transmission modes or the packaging requirements. Moreover, although it is desirable that the photolithographically defined spacings between the transmit and receive pairs are preferably small, of course larger spacings can be easily accommodated by the present invention.

Those of skill in the art will recognize many advantages of the second preferred embodiment of Figure 5a is that a typical process used to create arrays of VCSELs, including the isolation implant commonly used to separate the individual VCSELs of the array, can be used to create arrays of VCSEL/p-i-n photodiode pairs. The additional steps required to build the p-i-n photodiode on top of the VCSEL process are negligible in cost. Moreover, the difference in the thickness of the two devices is also negligible for purposes of facilitating near-field coupling of the devices to fibers to eliminate the need for optics. Additionally, due to the underlying second mirror of inoperable VCSEL 91, any light not absorbed by the intrinsic layer 102 of p-i-n photodiode 90 will be reflected back into intrinsic layer 102, thus having a second chance to be absorbed. Finally, the thicker the intrinsic layer 102, the lower the capacitance of the p-i-n diode 90 (the faster its operation) and the better its optical efficiency.

Figure 6(a) illustrates how the commonly used single fiber round ferrule can be implemented using two or more fibers. Such fibers are now currently available from Siecor as prototypes. The cylindrical ferrule 110 has the same dimensions (i.e., 2.5 mm) as those ferrules commonly used with only one fiber. Thus, one fiber 112 can be used for transmitting data as coupled to a VCSEL while fiber 114 can be used to receive data from a remote transmitter as coupled to a photodetector.

Figure 6(b) illustrates a commonly available rectangular ferrule which can have eight or more fibers 122, and which has guides 120 for receiving alignment pins. Rectangular ferrule 116 typically has a polished face 118 for coupling to an array of transmitting VCSELs. This rectangular ferrule 116 can be easily adapted to devices made in accordance with the present invention, such that each pair of fibers 122 can be aligned with a pair of integrated VCSEL/photodetectors.

Figure 7(a) illustrates how a single VCSEL /photodetector pair could be packaged using standard lead-frame technology to be interfaced to a rectangular multifiber ferrule such as the one illustrated in Fig. 6(b). Integrated transmit/receive chip 130 can be epoxied to lead frame 128 and then bonded to bond pads 141 via bond wires 143. If optics are required, lenses 138 and 136 can be formed over VCSEL 89, 92 and photodetector 62,90 respectively, either using materials which are formed over chip 130

during the manufacturing of chip 130 or such optics can be integrated within the surface of the plastic encapsulation formed by the package. Lead frame 128 can also have guide pins 140 to be used in conjunction with a rectangular ferrule such as the one shown in Figure 6(b). Figure 7(b) shows a side view of Figure 7a to illustrate the use of optics over photodetector 62, 90 and VCSEL 89, 92.

Figure 7(c) illustrates how lead frame 128 can be butt coupled to a rectangular ferrule 150 containing two fibers 124 and 126. If distance 160 is fairly precisely known, and distance 147 between fibers 124 and 126 is fairly precise, a fairly accurate alignment can be achieved between fibers 124 and 126 and VCSEL 89, 92 and photodetector 62, 90 because the distance between VCSEL 89, 92 and photodetector 62, 90 are fairly precise based on the photo-optical alignment process used in manufacturing the [integrated semiconductor] chip 130. Thus, a fairly accurate positioning of the chip 130 with respect to the lead frame 128 during packaging will provide a reasonably accurate passive alignment. Of course, fine alignment can be achieved using well-known active alignment techniques. A further advantage of the coupling technique shown in Figure [8] Z is that no optics must be interposed between package [146] 128 and ferrule 150 if the coupling distance 152 is close enough. Of course, a flat transmissive surface 148 can be easily achieved on package [146] 128.

Fig. 8 illustrates a lead-frame package which can be used to interface with a round multifiber ferrule such as the two fiber ferrule of Fig. 6 (a) Barrel 127 is designed to precisely mate with the round ferrule of Fig. 6(b).

**ATTACHMENT B**

Amended Claims with markings to show the revisions made.

22. (Amended) A monolithic optical transmitter and receiver pair comprising:  
a semiconductor substrate;  
an optical transmitter formed on a portion of said substrate; and  
an optical receiver formed laterally adjacent to said optical transmitter, said optical receiver optically and electrically isolated from said optical transmitter.